

FIG. 1

Station Groups for Execution Resource Sharing

- 8 ML Active Stations
- 8 DEE Active Stations
- 2 ML columns
- 2 DEE columns
- 4 sharing groups

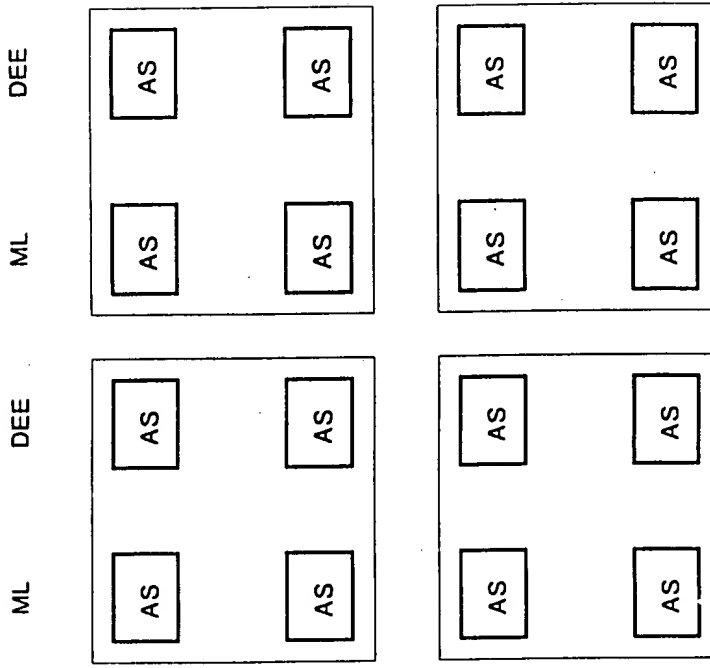


FIG. 1

High-level block diagram

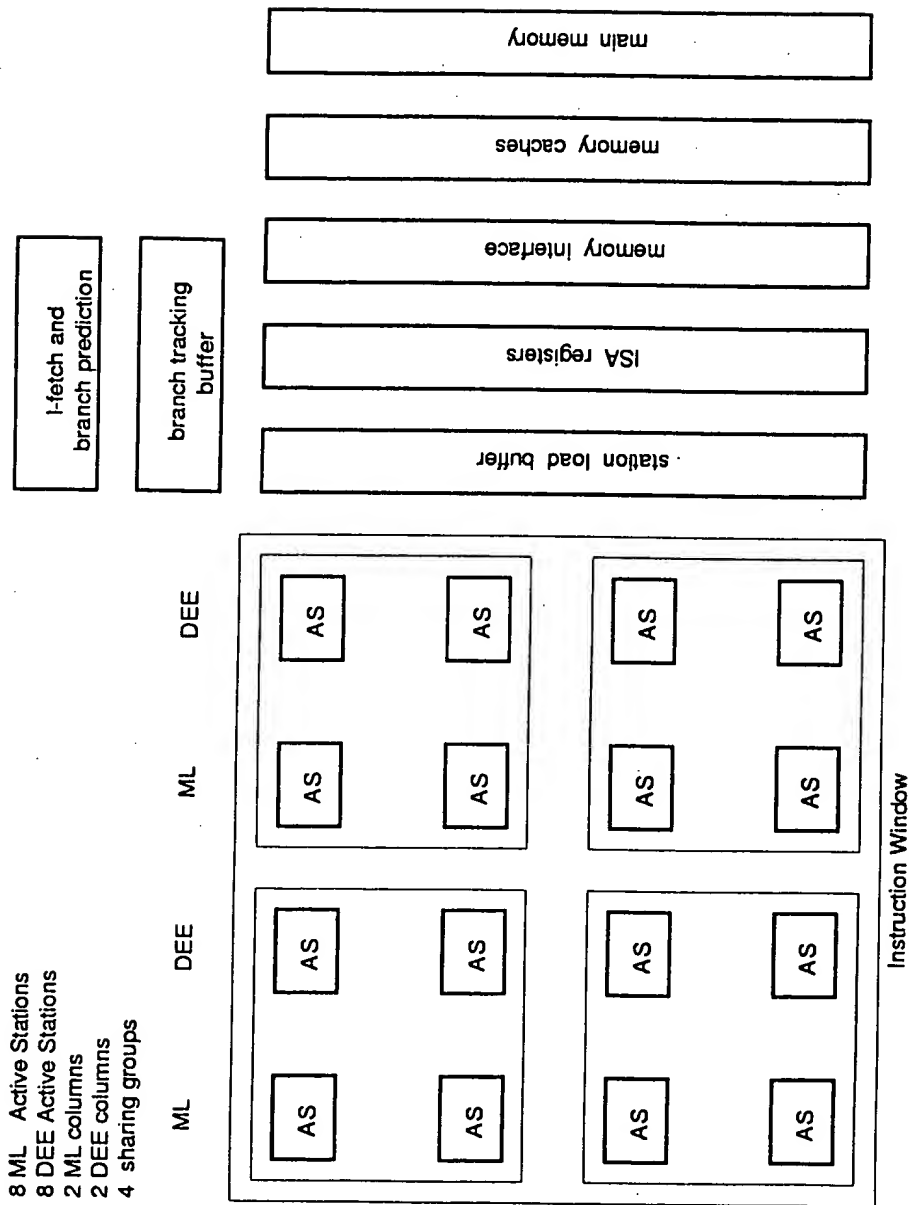


FIG. 2

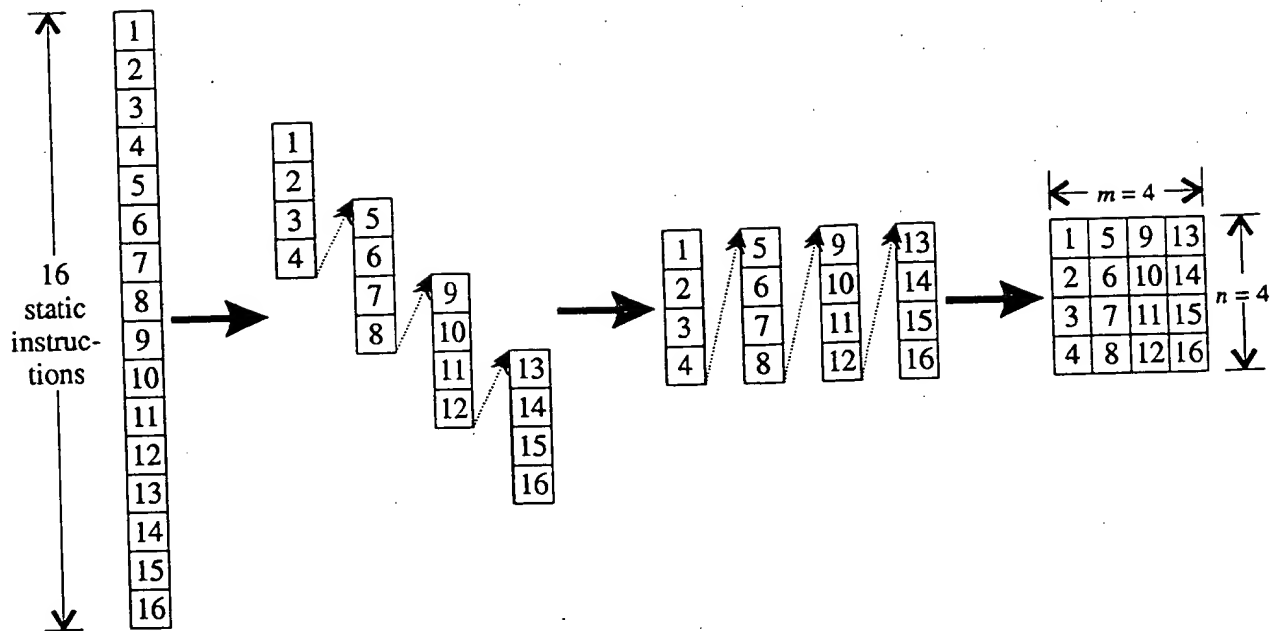
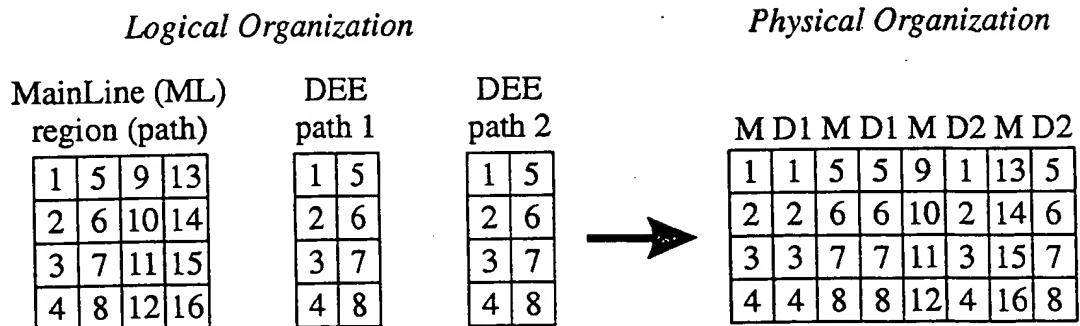


FIG. 3



Instruction Window (IW), with Disjoint Eager Execution (DEE)

- each square is an active station -

FIG. 4

ISA Architected Register Files

- 8 ML Active Stations
- 8 DEE Active Stations
- 2 ML columns
- 2 DEE columns
- 4 sharing groups

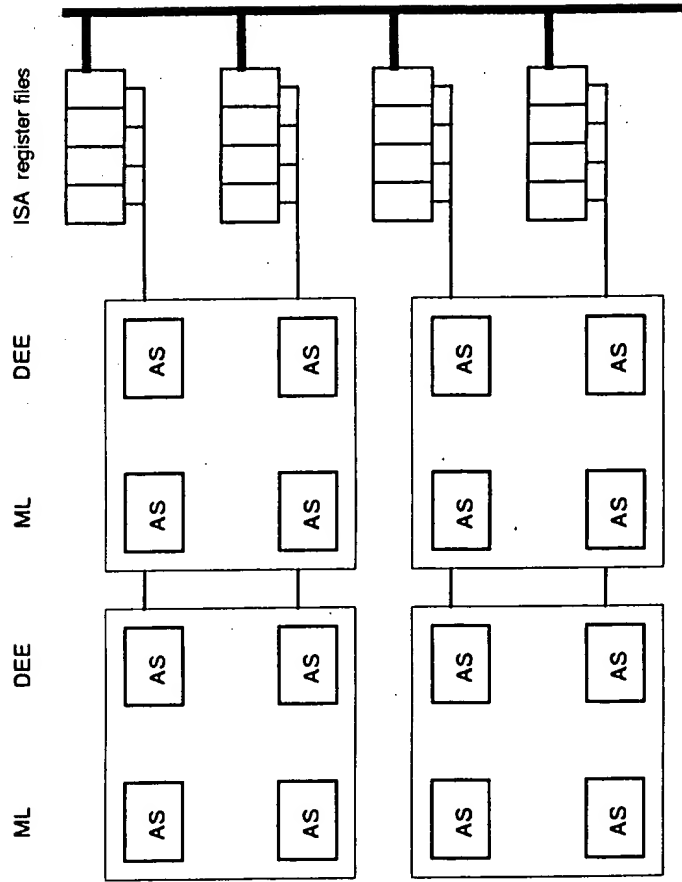


FIG. 5

Memory Interface and Buffers

- 8 ML Active Stations
- 8 DEE Active Stations
- 2 ML columns
- 2 DEE columns
- 4 sharing groups

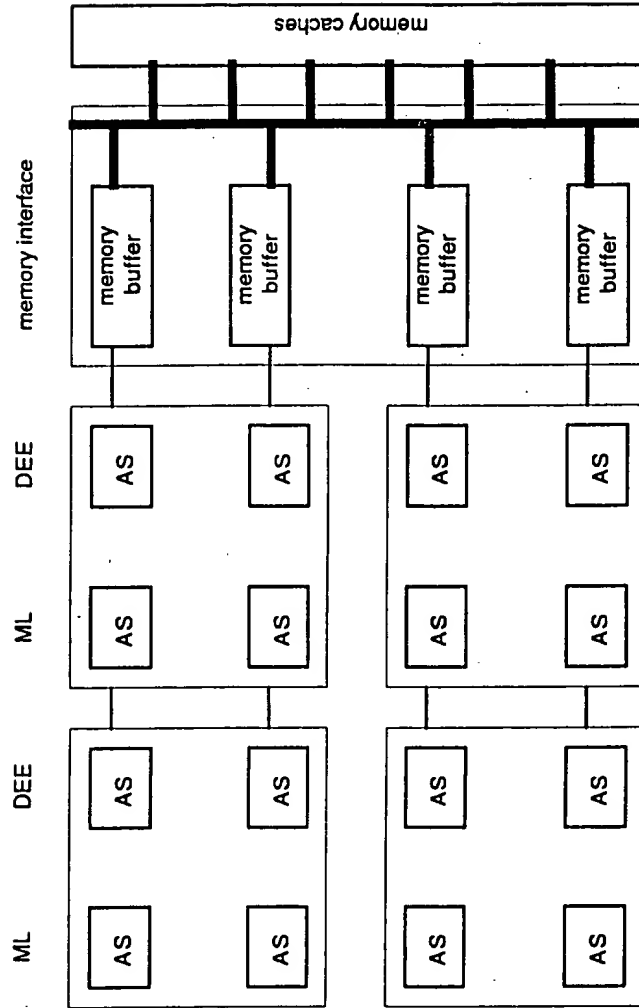


FIG. 6

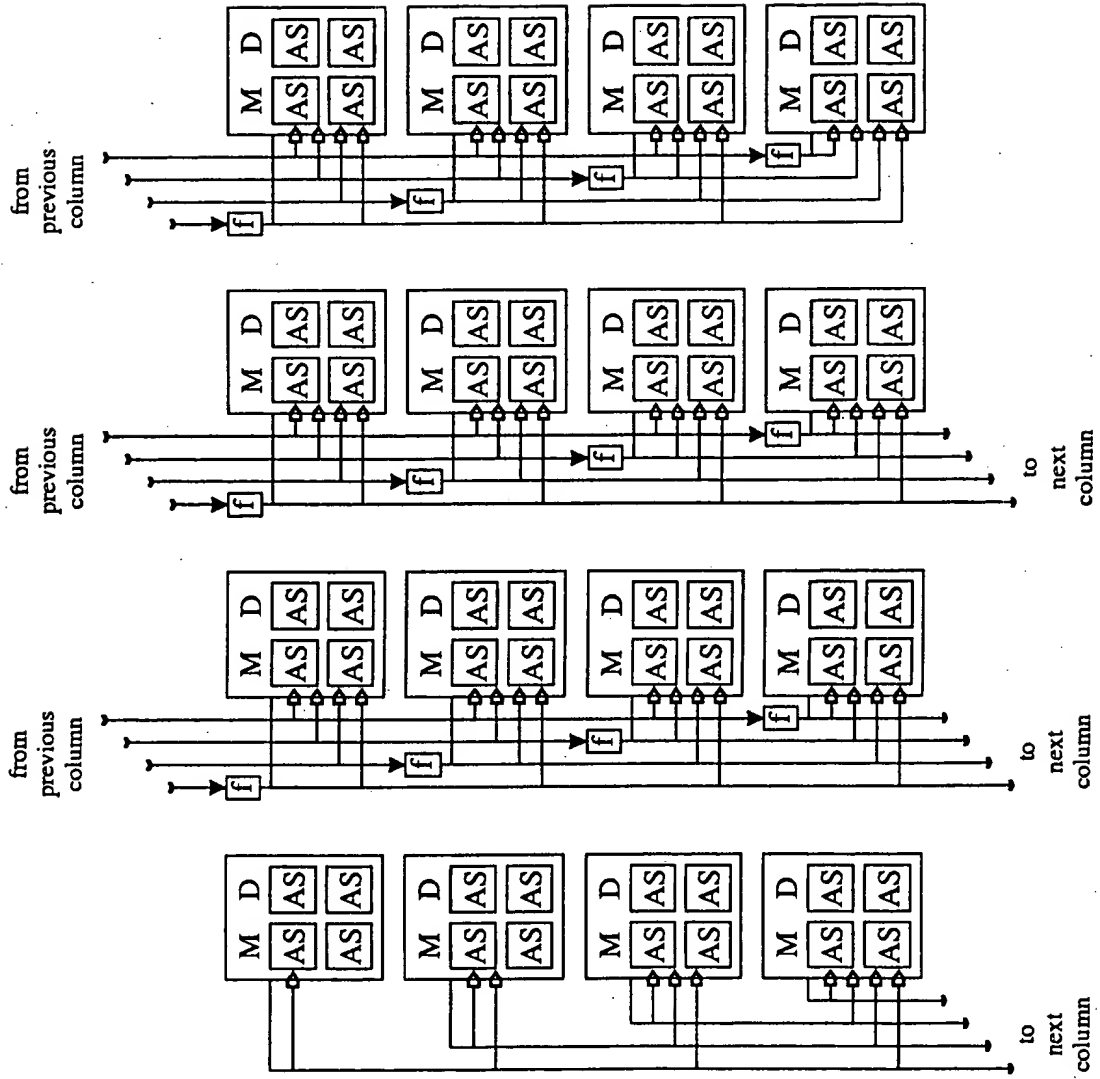


FIG. 7

Active Station Sharing Group and Connectivity

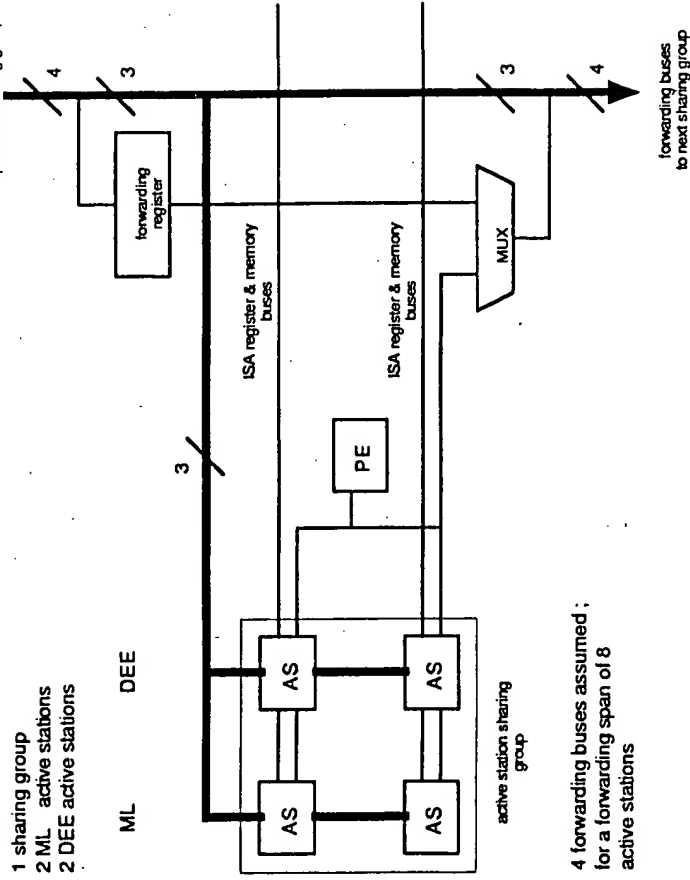


FIG. 8

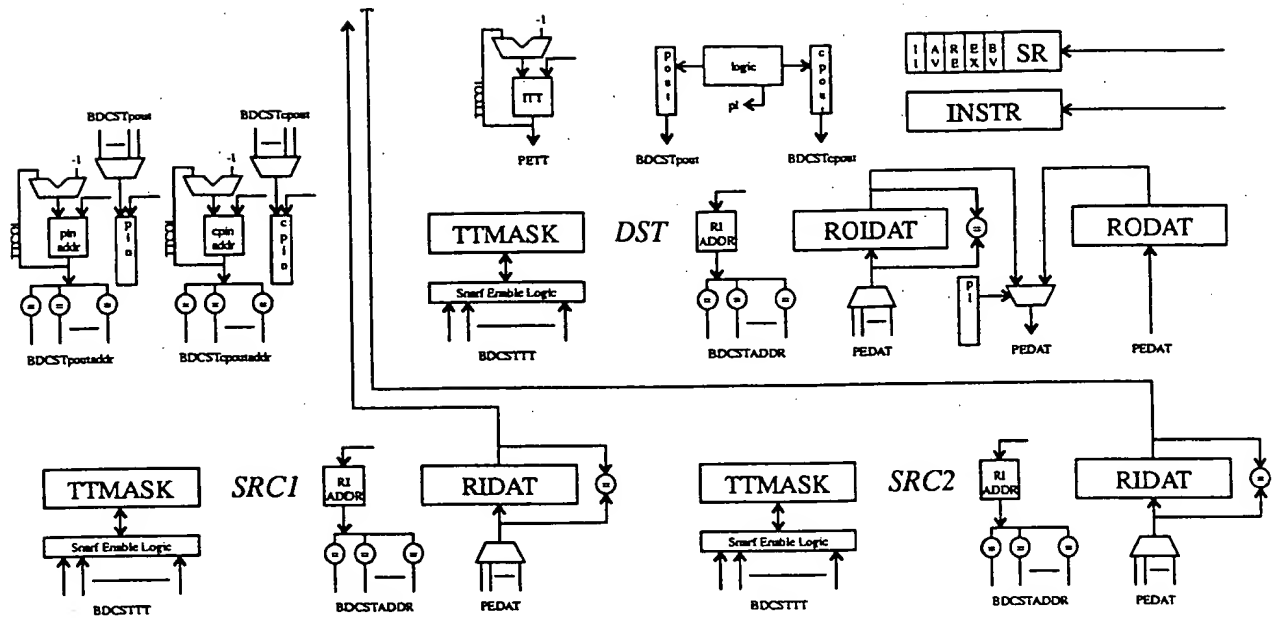


FIG. 9

ISA Register File Detail

two register files shown ;
two registers shown per
register file

register transfer
and column contention buses
for each register

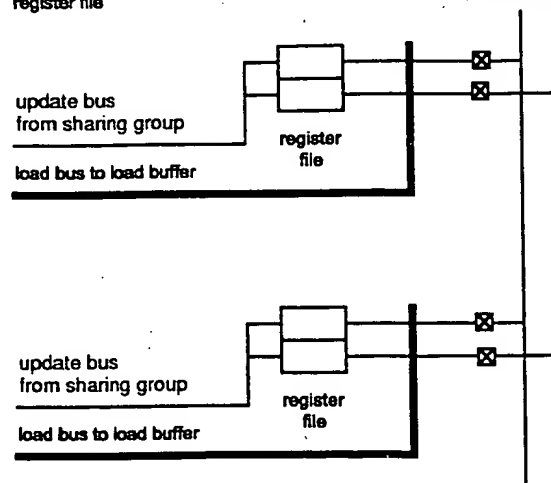


FIG. 10

instruction	time					
	00	X				
	10	X				
	20	X				
	30	X	X			

an 'X' marks an execution

FIG. 11

instruction	time					
	00	X				
	10	X				
	20			X		
	30		X		X	

an 'X' marks an execution

FIG. 12

instruction	time					
	00		X			
	10	X		X		
	20	X				
	30					

an 'X' marks an execution

FIG. 13

		time						
		0	1	2	3	4	5	6
instruction	00		X				X	
	10	X		X				X
	20				X			
	30		X	X		X		

an 'X' marks an execution

FIG. 14

	time						
	0	1	2	3	4	5	6
000	X						
010	X		X				
020	X			X			
030	X				X		

	time						
	0	1	2	3	4	5	6
00	X						
10	X	X					
20	X		R				
30	X						

		time						
		0	1	2	3	4	5	6
Instruction	00			X				
	10				X			
	20	X				R		
	30		X				X	

	time						
	0	1	2	3	4	5	6
Instruction	X				X		
00							
10	X	X				X	
20	R		D				B
30	X						